A Literature Review of On-Chip Network Design with Dynamic Reconfiguration.

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Abstract —— The architecture for on chip network design using dynamic reconfiguration is a solution to Communication Interfaces, Chip cost ,Quality of Service, guarantee flexibility of the network. The proposed architecture dynamically configure itself with respect to Hardware Modules such as routers, Packet based Switch and data Packet size by changing the communication conditions and its requirements at rum time. In Noc, we are using Hexagonal node pattern to improve the communication performance. The proposed design avoids the limitations of bus-based interconnection schemes which are often applied in partially dynamically reconfigurable FPGA designs. With the help of this design we can achieve Low latency and high data throughput. In this paper we are reviewing the previous methods and approaches of Dynamic reconfiguration in NOC.

IndexTerms — On chip Network, SOC, FPGA, NOC, Router, NI, PE, Dynamic reconfiguration.

I. INTRODUCTION

As everyone knows, developments in semiconductor technology have made very complex large scale System-on-Chip (SoCs) design available. Usually, in a System-on-Chip, interconnection between different Intellectual Property (IP) cores is achieved by means of shared bus architectures. However, now adays each new SoC generation integrates more processing elements (PE), new features and more new functionalities. With this increasing complexity, the system maybe needs extremely high capability in computation and communication. So, it is obvious that we can't continue to use shared bus architectures, which will affect performance of the overall system. Also, they can't present a scalable solution to existing problems in the communication.

In order to solve these problems, on-chip point-to-point distributed interconnection networks or Networks on a Chip (NoCs) have been proposed. Unlike the shared bus architectures, the key communication method in NoC

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Architecture is to implement interconnections of different IP cores using on chip packet-switched NOC. NoCs are mainly contains three major parts: Routers (acts as switches), Links and Network Interfaces (NI). In Network, Routers are the major part in Network and it precedes switching elements that are responsible for forwarding data packets from one router to another router using Different routing Algorithms. Links are acts as wires and it connects between different routers, and they are usually bidirectional. Network Interfaces are the wrapper between the router and processing element (PE). They have two different communication operations. Firstly, NIs can collect the data from all different kinds of elements that are attached to them, packet size, add the header data, source and destination address and tail data and send the processed packet into the attached router. Secondly, they receive the packets from the attached router.

This paper is organized as follows. Section 2 follows the literature review of different approaches and methods for on chip network design. The dynamically reconfigurable on chip Network using Packet switching method is explained briefly in Section 3. Section 4 tells about the conclusion of the paper.

II. LITEREATURE REVIEW

A Network-on-Chip (NoC) architecture that enables the network topology to be reconfigured. The architecture thus enables a generalized System-on-Chip (SoC) platform in which the topology can be customized for the application that is currently running on the chip, including long interface and direct interface between IP-cores. The interface is inserted as a layer between routers and wires, and the architecture can be used in combination with previous NoC routers, making it a general efficient architecture. The network topology is configured using energy-efficient topology switches based on physical circuit-switching as found in FPGAs. ReNoC architecture that enables the network topology to be reconfigured using energy-efficient topology switches. The

architecture was evaluated by mapping an application to a static 2D mesh topology as well as ReNoC architecture in two different topology configurations. The architecture consumes less power, when they configuring an application specific topology, compared to the static 2D mesh topology. The topology switches increased the area of the NoC architecture [1].

In paper [2], a run-time reconfigurable NoC framework based on the partial dynamic reconfiguration capabilities of Field-Programmable Gate Arrays (FPGAs). This new NoC framework can dynamically create/delete express lines between SoC components (implementing dynamically circuit-switching channels) and perform run-time NoC topology and routing-table reconfigurations to handle interface congestion, with less performance overhead. They proposed a NoC reconfigurable framework that can reconfigure the NoC topology at run-time, as well as enabling path reconfiguration and express lines creation/removal, while introducing an overhead on average of 10% of an initial static NoC design. They proved reduction in latency and increase in frequency.

With an increasing trend to implement Network-on- Chip (NoC)-based Multi-Processor Systems-on-Chips (MPSoCs), NoCs need to have guaranteed services and be dynamically reconfigurable Many current NoCs consume too much area and cannot support dynamic reconfiguration. In [3], presented an area-efficient Spatial Division Multiplexing (SDM)- based NoC. They replaced area consuming 32-bit to M-bit serializers with 32-bit to 1-bit serializers in the network interface and incur almost no loss in performance. In Their Detailed architecture for the NI and router which achieved area savings of more than 95% and improved scalability. Performing link allocation during design-time allows us to provide throughput guarantees as well as to generate different programming files for different use-cases which are used to dynamically configure the NoC during run-time.

The CuNoC (Communication Unit NoC), a new paradigm for intercommunication between modules dynamically placed on chip for FPGA based reconfigurable network devices. The CuNoC is based on flexible communication unit allowing a dynamic communication infrastructure which is namely adapted and suited to reconfigurable devices. The CuNoC can be adapted with small modifications to all others systems need performant communication medium. CuNoC is that allows a scalable network structure, a simultaneous communication with a good compromise between the logic area and operating frequency [4].

In paper [5] introduces and describes a novel reconfigurable communication infrastructure for dynamically reconfigurable architectures. They proposed approach is a tile–based Network–on–Chip in which the communication layer is completely decoupled from the computational one. It is designed to support dynamic reconfiguration at the communication fabrics level.
The use of the Network–on–Chip paradigm in the design of communication infrastructure for dynamically reconfigurable architectures as a suitable approach to guarantee flexibility and adaptability to the run time application changes. The routing mechanism has been done dynamic by directly reconfiguring the content of the BRAM blocks, storing the information about the routing path from the sender to the receiver end–points. In this way, a dynamic routing mechanism has been realized, in which the routing information relies on the current network status.

Due to their layered approach, Networks-on-Chip (NoC) are a promising communication backbone in the field of heterogeneous dynamically reconfigurable systems. In [6], a future FPGA architecture is discussed having a hardwired NoC as an additional high-level routing resource. Instead of implementing NoC interface with valuable reconfigurable hardware modules, on top of this architecture, low cost statically and dynamically reconfigurable systems can be built. Their model not only implements the NoC but also permits a tile based dynamic reconfiguration.

DyNoC has been presented [7] as well as a routing methodology able to handle obstacles in the network. The architecture can be used as communication medium in reconfigurable devices to solve the problem which arises when dynamically placed components need to communicate.

In papers [8][9], the adaptive reconfigurable multiprocessor Noc is configured dynamically with best parameters includes new routers, packet size and new efficient switching techniques. They described how reconfigurablity is processed in Smart Network Stack (SNS) includes network control and its simulations, exchanging the data at high speed and formation of circuit between two processing elements in efficient manner.

The bus based interface dynamically Reconfigurable with NoC is designed in paper [10] for low cost applications. They are taken core interface model as API Signal for communication bus , router design taking input from IP Cores. The high level platform architectures includes ARM7 Processor, Reconfigurable FFT and Veterbi decoder, SDRAM

and Memory controller. The core interface model and platform architecture acts as a bus interface model to NoC. They configured dynamically with above bus interface model to reduce design time.

The paper [11], the SoC Architecture is able to run with new protocols and task applications. The NoC Architecture dynamically reconfigure with host controller permanently or temporarily. They are using dynamic routing algorithms to find out the tasks in NoC Platform. Because of this they can control or tolerate faults in NoC.

III. DYNAMICALLY RECONFIGURABLE PACKET-SWITCHED NOC

The Dynamically Reconfigurable module mainly consists of Packet switching and and NoC Design modules. The main architecture as shown in the figure 1.

Firstly receiver module receives the data serially like FIFO and gives to RAM. The RAM stores the data in address locations. if data is valid, analyzer analyses the data in the form of packet send it to the NoC.

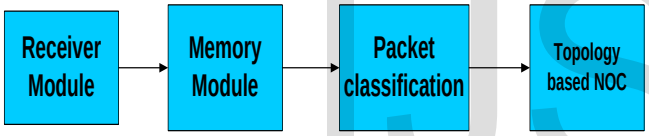

Figure.1 Flow of Dynamically Reconfigurable Packet-Switched Network-on-Chip

The NOC mainly contains routers, hardware module and I/O buffers. Apply Dynamic adaption concept for NOC as shown in figure 2.

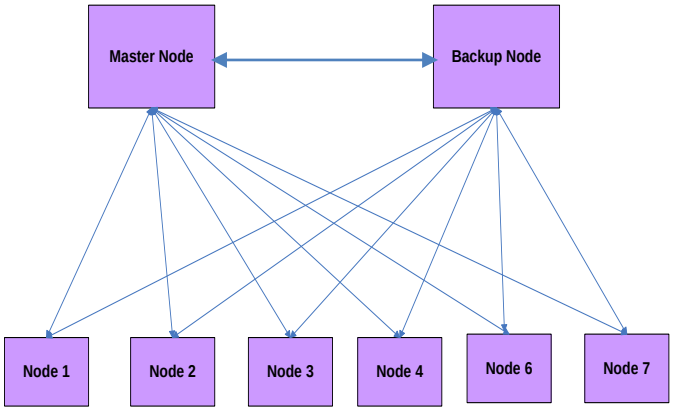

Figure.2. Dynamic adaption of the NoC while failure of master hardware modules.

When there is a failure the structure of a NoC special care has to be taken not to isolate parts of the NoC and to make sure that failure is not going to affect the communication among the node. A typical scenario is depicted in figure 2. Here, a hardware module (Master Module) is pretended to be failed and is no more efficient to perform the process of switching the data between the node and need to be replace by the new one which fit in the same area. As for the new configuration a connection port for master node to the NoC is missing, a new module has to be inserted to get communication back in action without affecting the present communication. Since the dynamic reconfiguration should not affect other hardware modules and their communication, it has to be guaranteed that no packets are sent directly from any node to receiver node through master module. Therefore, routing tables of switch nodes are temporary updated in an order that the communication is established with the help of Backup node. Once the new master node is reconfigured the once again the nodes are updated with the new master node address to perform in regular manner.

In addition, the node are to be designed in hexagonal pattern in order to provide more information and proper device utilization. The routing table of switch should hold information to access the new switch. These updates are done by means of internal NoC-packets containing the routing tables of the neighbor switches. These packets are sent by the global control unit of the system. The switches are addressed by a physical address in the header of the packets, while for the hardware modules logical addresses are provided. The internal NoC-packets are marked highest priority, ensuring that they are processed immediately by the packet-switched NoC. During dynamic reconfiguration it is assumed that the connections between switchs are not affected.

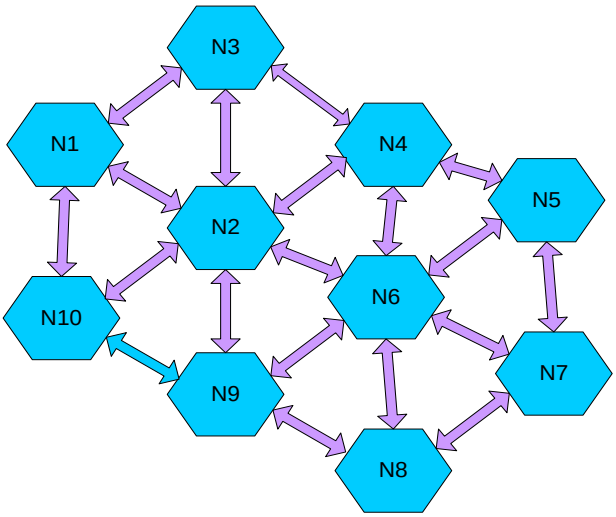

Figure 3. Hexagonal node pattern to improve the communication performance.

I. CONCULSION

In this Paper we are discussed about different approaches for dynamically reconfiguration in on chip Network architecture. When we are replacing the hardware modules, so we need to follow the constraints includes initial conditions, packet size, topologies, , our main approach is to avoid the communication failures between the networks and also speeds up the network process,low latency and high data throughput.

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